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# ASIC IMPLEMENTATION OF THE SYMMETRIC FUZZY PROCESSOR AND ITS APPLICATION TO ADAPTIVE SYSTEMS

by

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**TO MY MOTHER**

**AND**

**FATHER**

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# ABSTRACT

This dissertation presents a VLSI design of a symmetric fuzzy processor. The design features fuzzification, defuzzification and inference operations while allowing the implementation of a knowledge base via rules. By combining the inherent advantages of symmetric triangular membership functions and fuzzy singleton sets, a novel structure for the fuzzification model is obtained. The structure accelerates the evaluation of the antecedent degree which is evaluated by a simple mathematical relation which calculates the resulting value using the end-points of matched fuzzy member functions. This feature enables the processor to avoid the requirement of storing all the sample values of the fuzzy membership function in memory as is the case with other approaches. In addition, the resulting design structure simplifies computations associated with centroid defuzzication in that certain simplifying assumptions eliminate the need for a divider circuit. By using a very high speed integrated circuit hardware description language (VHDL) compiler and by making use of a simulator provided through the Mentor Graphics EDA design tool, optimization of the VLSI design has been obtained. Results show that the resulting fuzzy processor can be implemented on a single 1.2μm CMOS VLSI chip with 16.7 $mm^2$ die size and a total of 36,080 transistors. Moreover, simulation indicates that numerical computations including centroid defuzzification can be accomplished in 0.55 μs. within an accuracy of 96%, thus making it suitable for a wide range of real-time applications. Up to 49 consequent knowledge rules based for seven fuzzy membership functions associated

with the chip's two input variables can be downloaded into a 64-byte static RAM allowing designers to create a fuzzy processing system without the need for additional on-board memory. Finally, as an example of the application of the proposed fuzzy processor model, results are presented from a study to simulate a second order linear control system and a non-linear structure for adaptive channel equalization of a bipolar signal passed through a dispersive channel in the presence of additive noise. It is shown that difficulties commonly associated with channel non-linearity and additive noise correlation can be overcome by the use of an equalizer employing the developed fuzzy structure.

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# CHAPTER 1

# INTRODUCTION

The applications of fuzzy set theory and fuzzy logic have increased and widely used in a variety of fields. To support the ever expanding applications of fuzzy systems, a hardware implementation of fuzzy logic is strongly desired. Consequently, dedicated VLSI hardware has been developed both in the form of digital and analog VLSI systems [11]-[29]. Moreover, recently recorded efforts [13]-[18] have combined the inherent advantages of analog and digital electronics in the development of fuzzy logic system (FLS) inference engines. However, the richness of parameters associated with FLS's often leads to complicated VLSI FLS chips [15]-[18], in which most utilize digital microprocessors or microcontrollers programmed with sequential calculations of fuzzy logic quantities. The drawbacks in this type of VLSI FLS chip are low speed, high cost, and long design time. Besides, an expensive development system is also needed to program the general purpose microcontroller chip for a specific fuzzy logic control system. Although some recent FLS chip hardware implementations [17]-[19] have low cost-effective design, they still require a large fuzzy memory due to their behavior of storing all the sampled values of membership functions for all universes. Consequently, this effectively hinders the speed of the hardware due to retrieving and evaluating the matched membership degree values. In addition, due to the lack of mathematical models

for the design of the FLS, most existing FLS chips [11]-[28] use very complicated fuzzy sets and membership functions in the hope of satisfying a variety of applications. Therefore, these FLS chips [11]-[28] suffer the drawbacks of high cost and long design time.

It has been shown in [32]-[38] that the FLS with center-average defuzzifier, product inference, and singleton fuzzifier is a universal approximator; i.e., for any given real continuous function g on the compact set U, there exists a fuzzy logic system such that it can uniformly approximate g over U to arbitrary accuracy. Therefore, the fuzzy logic systems with the features mentioned above are qualified for use as building blocks for adaptive nonlinear systems. Furthermore, using some specific functional form for membership functions; i.e., symmetric normalized triangular membership functions, the fuzzy logic systems given may be simplified to the form expressed in our earlier paper [2] which also was proven in [2] to be a universal approximator of arbitrary accuracy. In addition, the fuzzy logic system described in [2] may be constructed from fuzzy IF-THEN linguistic statements using specific fuzzy inference, fuzzification, and defuzzification strategies. Therefore, linguistic information from human experts can be directly incorporated to the systems. Herein, we present our fuzzy processor module which incorporates the following features:

- two singleton inputs,
- one crisp output,
- seven symmetric triangular membership functions associated with each input,

- 64-byte static RAM for consequent knowledge rule-base storage, and
- on chip fuzzification and defuzzification processes.

The implication and inference operations are evaluated using product operators where the defuzzification scheme is accomplished through the evaluation of a fuzzy centroid equation which has been shown to be well-suited for application to engineering problems, [35]-[38]. One should realize, that even though the parameters of the structure are limited in terms of its inference operations, the shape of its fixed membership functions, and its reliance on centroid defuzzification, the structure itself is capable of supporting a wide class of applications [2]. A typical use of the structure will be demonstrated in Chapter 4.

The following chapters outline the major structure operations including fuzzification, the implementation of knowledge rules, inference, and the defuzzification scheme. Chapter 2 presents a brief introduction of fuzzy set theory, in which basic definitions and operations in fuzzy set theory are introduced. Also, it includes a detailed description of fuzzy systems, in which we introduce our symmetric fuzzy system structure and demonstrate its mathematical operations. This chapter also details the operations and the features of our symmetric fuzzy processor. Chapter 3 presents a VLSI implementation of the processor using a VHDL compiler and logic simulator through Mentor Graphics, followed by a detailed examination of the chip's silicon area, delay time, critical path, clock cycle, accuracy, and several simulation examples. In Chapter 4, as an example of the chip's applications, the structure is applied to several control problems as well as to a non-linear intersymbol interference channel equalization problem. Moreover, the

hardware is interfaced with a C code program to achieve control and the results are presented. Finally, Chapter 5 discusses the results from current efforts and recommends future research. The VHDL code for our circuit as well as a C code for our fuzzy model are presented in Appendices A and B, respectively.

# CHAPTER 2

# PROCESSOR MATHEMATICAL STRUCTURE

## 2.1 Introduction

Most of the fuzzy logic (FL) literature deals with mapping from fuzzy sets into fuzzy sets (we will define and illustrate what is meant by fuzzy set later in this chapter.) In many applications of FL to engineering problems, we are interested in mapping from numbers into numbers, and not sets into sets. Consequently, our problem is more difficult than the usual FL problem. In order to accommodate applications such as intelligent control, we have to add a front-end "fuzzifier" and a rear-end "defuzzifier" to the usual FL model. The resulting framework is called a fuzzy logic system (FLS). The purpose of this chapter is to show how to interpret the nonlinear mapping of an FLS geometrically as is commonly done in FL engineering applications, and also how to write a detailed formula for its input-output relationship. In general, an FLS can be implemented in an enormous number of ways yielding numerous different mappings. This requires a careful understanding of the FLS structure and the elements that comprise an FLS. Therefore, we present our FLS mathematical structure which limits the number of possibilities, but does so in such a way that we retain the ability to cover a wide class of applications. Later in Chapters 3 and 4, we will discuss the parameters associated with the FLS and how they indeed lead to its ability to accommodate numerous applications.

### 2.2.1 Definitions Associated with Fuzzy Sets

Some of the basic definitions used in fuzzy set theory [3]-[6] are introduced in this section.

(1) A *fuzzy set* ,A, is defined in a universe of discourse, X, *by its membership function* which associates each element $x_i$ of X with a degree of membership grading $m_i$. Here, the fuzzy set A is considered as the union of its constituent *singletons.*

$$A: X \rightarrow [0,1],\ X = \{x_1, x_2, \ldots, x_n\}, \tag{2.1}$$

$$A = \{m_1 / x_1, m_2 / x_2, \ldots, m_n / x_n\}, \tag{2.2}$$

The *height* of fuzzy set A is defined as the supremum of its membership function:

$$\text{hgt}(A) = \sup_{x \in X} m_A(x). \tag{2.3}$$

(2) A fuzzy set, A, is said to be *normal* if its height is unity; otherwise, it is *subnormal*..

(3) Two fuzzy sets, A and B, are said to be equal (A=B) if and only if

$$\forall\, x \in X,\ m_A(x) = m_B(x). \tag{2.4}$$

(4) For two fuzzy sets, A and B, we say A *is contained* in B ( $A \subseteq B$ ) if and only if

$$\forall\, x \in X,\ m_A(x) \leq m_B(x). \tag{2.5}$$

(5) A fuzzy set, A, is a *subset* of fuzzy set B ( $A \subset B$ ) if and only if

$$\forall\, x \in X,\ m_A(x) < m_B(x). \tag{2.6}$$