EVALUATION OF IMPLEMENTING A NOVEL MODULARLY CONFIGURABLE ATTACHED PROCESSOR ARCHITECTURE USING GAAS DCFL TECHNOLOGY

SRINIVAS R. MARAM

Department of Electrical & Computer Engineering

APPROVED:

Dr. Vijay P. Singh, Chair

Dr. Glenn A. Gibson

Dr. John C. McClure

Associate Vice President for Research and Graduate Studies

To my Parents.

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by

SRINIVAS R. MARAM,B.E.,M.E.

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ABSTRACT

The interaction between computer architecture and integrated circuit(IC) technology is complex and bidirectional. The characteristics of various implementation technologies affect architects' decisions by influencing performance, cost, and other system attributes. Developments in computer architecture also impact the viability of different technologies. The implementation requirements of various architectures can emphasize different technology characteristics such as density, power, and speed.

To understand the interaction between computer architecture and IC technology, and the attractiveness of a technology for use in computers, we need a metric to evaluate different computer designs. In designing a computer today, the most important considerations are usually speed and cost. Secondary metrics, which may vary in importance, include power, size, cooling, and noise.

In this thesis, an assessment of a novel MCAP architecture using GaAs technology is made based only on the performance. Many of the secondary factors are indirectly measured, while some are difficult to quantify.

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CHAPTER 1

INTRODUCTION

1.1 Computer Architecture

Performance of a given architecture, whether it is RISC, superscalar, or super-pipelined, is always limited by interconnection delays when programs must obtain data over long interconnections from remote places. Improvements in the Performance of any architecture can be achieved by

* Building processors together with sufficient local memory to sustain performance. Performance will be lessened in proportion to the frequency of access of remote data by the Processors.

* Processor performing other tasks instead of waiting for remote data when it is needed.

* Fetching data into the local memory of the Processor by control units before it is needed. [1]

If all of the above are taken care of, then the performance will be limited by the clock rates of VLSI chips or Multichipmodules (MCMs). As the dimensions are very small and as the reflections die out quickly clock rates of a few gigahertz are obtained within a chip or between the chips on a MCM.

One way of estimating the performance of a given computer system is by evaluating the number of instructions executed per second; for example millions instructions per second

(MIPS). This can be improved by reducing the average number of instruction execution cycles and lessening the machine cycle time [2]. Tables 1.4, 1.5 and 1.6 [3] show the performance of some of the current high performance computers. The instruction execution cycle is determined by the architecture of the system. However, machine cycle time depends on VLSI and packaging technology. Hence, in order to increase the systems, speed, integration scale of VLSIs and the packaging density of electronic equipment had to be enhanced.

In Chapter 2 a novel Modularly Configurable Attached Processor has been discussed which attains its quickness and high utilization by:

*Closely matching its architectures to the set of algorithms it has to execute.

*Processing and memory accessing by using memory prefetching simultaneously.

* Minimizing the movement of data.

* Using high speed GaAs technology with MCM or WSI. [4]

Advanced Packaging technologies namely, MCMs and WSI are described in detail in Chap.3. The key is to partition computations so they rely mostly on local data. Paradigms such as global memory, message-passing, and hardware cache-coherence can permit any needed non-local exchange. Although these schemes have relative costs and performance penalties, when interconnection time limits performance, no scheme will help unless remote data access occurs. Programs must be structured to be mostly local to reach new levels of performance. Hence, to take advantage of the increased performance allowable by advanced interconnection technology, the processor organization must be designed in tandem with the interconnection technology.

1.2 Interconnection & Packaging

The continuous increase in chip integration, higher complexity of electrical modules, advances in printed circuit board technology and application of miniaturized and high pin count component packages have been utilized over the last few years to increase the processing performance. VLSI gate arrays with 10,000 plus gates and a gate delay of less than 100 pS are used in present mainframe designs. The packaging systems have been changed from card-on board system to a planar system where multichip modules are the performance criteria for high end mainframes.

The principal motive for building transistors out of gallium arsenide (instead of the ubiquitous silicon) is speed and more speed-either higher maximum frequency of operation or higher logic switching speed. This outcome is to be expected because of the superior electron dynamics of n-type GaAs. GaAs is a much more difficult material to work with in semi-conductor manufacturing. GaAs is a binary compound (one atom each of gallium and arsenic). This fact lies at the root of many of the technological obstacles to utilizing the III-V compound in electron devices.

1.3 Gallium Arsenide:

GaAs is emerging as the starting material for the integrated circuits with one million or more transistors per chip[5]. The technology today is firmly in the domain of high-performance, very large scale integration (VLSI), with chip clock rates hitting 100 MHZ and

up. And to cap everything, the manufacturing cost is reasonable. Table 1.1 illustrates the volume of business that has been done commercially. One of the most prominent applications of GaAs technology is in ultra-high speed digital integrated circuits design for supercomputers. Circuits as complicated as 16*16 bit multipliers, 1K SRAM, 4K SRAM, 16K SRAM, 64K gate arrays have been built, and GaAs medium-scale integration (MSI) ICs have been fabricated with reasonably good yields. GaAs MESFETs were first introduced as discrete devices for microwave applications in the late 1960s. It was not until 1974 that Rory Van Tuyl and Charles Liechti of Hewlett Packard first reported the use of MESFETs for digital applications. The first integrated circuit was a simple NAND/NOR gate that was configured as buffered FET logic (BFL). This circuit used about five transistors and a few level shifting diodes and achieved performances down to about 100 pS of propagation delay. In 1977 Van Tuyl et al. reported a frequency divider circuit that operated at 4 GHZ. This integrated circuit was based on liquid phase epitaxy technology, and it consumed a large amount of power, about 20 mW per logic gate. However, its speed performance stirred a worldwide interest in GaAs digital circuits. In 1978 Richard Eden and coworkers at Rockwell International reported an improved circuit known as schottky diode FET logic (SDFL) in which the power hungry level shifting circuit in the BFL output level shifter was replaced by very small diodes at the SDFL gate input. These diodes performed the dual function of level shifting and logic implementation and considerably reduced the power consumption per gate. The power consumption came down by an order of magnitude to a few milliwatts without sacrificing speed, and the simpler circuit had the added advantage of packing density. The epitaxial growth process was replaced by ion-implantation which offered much better uniformity and

reproducibility. By 1980 the Rockwell team had taken the SDFL approach on ion-implanted material and had demonstrated the first GaAs LSI circuit in the form of an 8*8 bit parallel multiplier with a complexity of just over 1000 logic gates.

In the early 1980s the depletion-mode MESFETs used in the logic circuit were gradually replaced by enhanced mode MESFETs. Logic gates built from the enhancement mode MESFET have compatible input and output logic levels without the need for level shifting diodes and so can be directly coupled to each other. Hence the term direct coupled FET logic (DCFL) was developed. The elimination of the level shifting circuits plus the virtue of very low logic swing of DCFL reduced the power consumption by a few hundred micro watts per gate. The elimination of level shifting circuits also helped to significantly simplify the circuit layout and consequently further increased the packing density. The development of self-aligned technology improved the GaAs device's performance. With enhancement-mode and depletion mode transistors placed on the same chip, circuit designers could now use DCFL to fabricate up to 30K gate array. This circuit structure reduces the chip area needed for a gate to about one-third that for an equivalent ECL gate. It has much higher speed capabilities and much less heat dissipation (about one quarter) than ECL devices. [5] Figure 1.1 compares the speeds and complexities of CMOS, ECL, and GaAs integrated circuits. Four-layer metal DCFL gallium arsenide processes use fourteen to sixteen mask steps, whereas comparable CMOS processes use 22 to 26 mask steps, and BiCMOS processes use 26 to 31. The smaller number of masking steps in GaAs tend to equalize the cost.

GaAs VLSI transistors are the off-spring of ion-implantation: ion beams impregnate the starting semiconductor material with dopants. They are field effect transistors wherein which

currents flow between their source and drain whenever a voltage is applied to their control terminal (gate), generating an electric field between the gate and the channel. The conducting channel is created by a separate implantation step in the GaAs device. Electrons forming the current pass a little beneath the conducting surface and thus the electron dynamic behavior of the buried channel device is ruled by the semiconductor's bulk properties. In the GaAs transistor, the gate electrode contacts the semiconductor surface directly forming a schottky diode between this terminal and the channel. The majority of near-term applications include high speed acquisitions and perhaps storage of very wide-bandwidth pulsed, pseudo random, or continuous stream data and its processing in real time. Generic areas for the application of these types of digital systems will be in military radar signal processing and signature analysis, electronic countermeasures and electronic support measures, and spread spectrum communications. Gallium Arsenide components can be profitably employed in the region of the data input (i.e., at the front end) of a signal processor confronted with a continuous stream of digital data. Such cases arise in computed tomography. These single, high speed streams must be partitioned into a set of lower rate parallel-substreams, which in turn can be further processed by silicon devices operating at much slower clock rates. Another application for GaAs integrated circuits operating at high clock rates arises in the implementation of certain type of algorithms that cannot easily be parallalized. The class of problems that can be executed in a straight forward manner with a single uniprocessor or with a small number of coprocessors, all operating at relatively high speed, includes certain types of iterative algorithms.