FREE-SPACE OPTICAL BUS ARCHITECTURE

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FREE-SPACE OPTICAL BUS ARCHITECTURE

by

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THESIS

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To

My parents

and

My husband, Floyd,

With all my love

Acknowledgements

I want to thank my husband, Floyd, for his constant support. I could not have finished without knowing he was behind me all the way.

I want to thank my parents for all the love and encouragement they gave me throughout the years. I wish they were with me today.

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Abstract

Multiple processor computers require interconnection networks for inter-processor and inter-memory communications. A common interconnection network is the computer bus. Traditional electrical buses have limited speed and bandwidth. Optical buses increase the potential for throughput by enabling pipelining of communications, increased bandwidth and, possibly, increased speed of communications. Two optical bus communities (fiber-based and free-space) exist side by side with little overlap.

This thesis proposes a reasonable architecture for a *Free-space Optical Bus (FSOB)*. This architecture bridges the two worlds of fiber-based and free-space-based research. An Architectural Framework Model (AFM) is proposed as a consistent method of describing an architecture. The AFM is used in the development of the FSOB architecture. This architecture addresses the following concerns: necessary physical volume, speed increase and potential increase of bandwidth. The proposed architecture is assessed and evaluated to show that this bus architecture can be configured to exceed the requirements of fiber-based optical buses.

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Chapter 1

INTRODUCTION

1.1 Overview

Multiple processor computers require interconnection networks for inter-processor and inter-memory communications. The simplest and most common interconnection network is the computer bus. A bus is usually implemented as one or more signal lines connecting all devices together. A signal transmitted by one device is received at all other devices [1]. Traditional buses used in most computer systems today allow only one communication at a time between any source and destination. Although many improvements have been implemented to increase the throughput of the bus, the computer bus is still a bottleneck that limits the computational potential of the system as a whole. This effect is more apparent in multiprocessor systems. The bottleneck occurs because all communications to and from each processor must take place via the bus. Only one processor can communicate at a time using a traditional bus.

In a multiprocessor system, it is often the case that processors must wait for data to be received before processing can occur. Processors may be idle until the data is

received. The quicker the data can be passed to the processor the less idle time and more computational time may exist. The same reasoning can be extended to include the ability to pass multiple messages during the same time frame.

The current technology for the computer bus is electrical. It is a proven technology and is the most widely used in the computer industry. Conversely, the electrical bus has several attributes that limit the growth potential of this medium. The first is the maximum speed that an electrical signal may achieve on a wire medium. The next is the fact that electrical signals propagate in multiple directions which disallows multiple electrical signals to exist without collisions.

Optical interconnects have the potential of alleviating the above issues. Light has a fast transmission speed. Also, light propagates in a single direction and has predictable path delays allowing pipelining of messages on a shared medium [2]. These properties allow for a faster transmission and for more than a single message to travel on the bus during the same time period. Combining this concept with free-space optics has the potential of multiplying these benefits. By removing the physical mediums mode of transmission, data speed and the number of interconnects can be increased.

1.2 Motivation and Objectives

There are several motivations for pursuing computer bus architectures with increased potential. First and foremost is the integral idea that increasing the communication potential between computer components will in turn increase the speed of the system. Second, optical interconnects have an untapped upper boundary in the area of speed and bandwidth that will have impacts on traditional areas of computer operations.

This thesis proposes a reasonable architecture for a Free-space Optical Bus. It is comprised of known or anticipated components and it expands on optical bus archi-

tectures proposed in literature. This architecture addresses the following concerns: physical volume necessary to implement, speed increase and the potential increase of bandwidth.

The physical volume necessary for implementation can be prohibitive with some transmission mediums. A message needs to reach its destination to be effective. Each destination has a unique address and several addressing methods exist to route the message to the correct location. These addressing methods are detailed in Chapter Two. Some addressing methods require separate and distinct pathways for the address and the message. Each pathway increases the amount of volume that the bus occupies. If fiber is used as the medium, the physical volume needed to implement would soon become excessive. In contrast, free-space optics will allow many data paths to be created in a relatively small volume.

The speed of the transmission between components is inherently increased simply because the mode of transmission is 'free space'. The speed of an optical transmission over fiber is approximately 200,000 km/s. The speed of an optical transmission through air is approximately 300,000 km/s [3].

The idea is to not only increase the communications speed between processors but also to increase the number of shared pathways. The bus will be expanded from a single link to an array of links between components. Using pipelining techniques, these pathways will be able to carry many messages simultaneously. It will increase bandwidth but minimize the physical volume requirement by using a shared bus space.

The proposed architecture will be assessed and evaluated to show that this bus architecture can be configured to exceed the requirements of fiber-based optical buses. The algorithms that are defined for a fiber-based bus should be transferable to the new architecture and the behavior should be comparable.

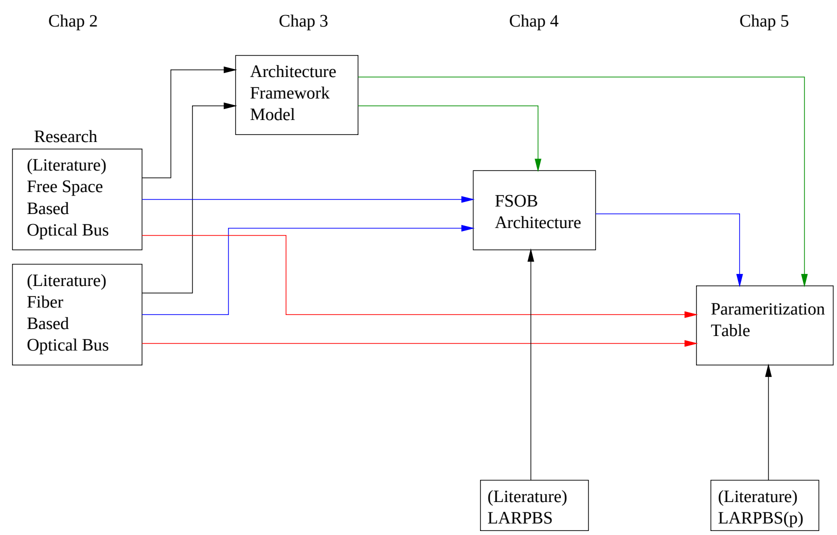

Figure 1.1: Chapter Overview

1.3 Thesis Overview and Organization

This thesis is organized into six chapters. Chapters three through five each describe a separate concept. The concepts presented in these three chapters are original and are each a separate contribution. Each chapter builds upon the ideas from the preceding chapters. The result is a specific architecture that is both developed and defended. The culmination of the ideas used to develop and defend the new architecture is a comprehensive way of evaluating existing optical bus architectures and guiding future architectures. Chapter six summarizes the concepts introduced in the thesis and describes future work. An illustration of the chapter design can be seen in Figure 1.1.

Chapter two provides a historical overview of various optical bus types, including both fiber-based and free-space-based. It also explores existing physical components that may be used to implement an optical bus architecture based on free-space.

Chapter three introduces a methodology for organizing and describing an optical bus architecture. An Architecture Framework Model (AFM) is proposed and the

levels are defined. Next, the AFM is applied to two example architectures taken from the literature. The first application is for the Integrated Free-space Optical Bus architecture. The second is for the fiber based Linear Arrays with a Reconfigurable Pipelined Bus System (LARPBS) model.

Chapter four describes Free-Space Optical Bus (FSOB) architecture. Three free-space architectures are described using the AFM. The first is based on a generic optical bus model. The second, the FSOB model, is based on a popular optical bus defined in the literature, Linear Array with a Reconfigurable Pipelined Bus System (LARPBS). The final architecture is a variant of the LARPBS architecture. Reasonable devices are described to show the viability of free-space optics on a mature fiber based model. In the course of this work, two devices, a delay device and a detector, were designed since an extensive literature and commercial products search failed to identify any suitable devices. This chapter concludes with a proof describing the inheritance of algorithms from the fiber-based architecture to the free-space-based architecture.

Chapter five defines an organizational method for categorizing the parameters used in describing a model and its associated architecture. It builds on an existing description given in the literature by integrating the AFM model and creating a technique for organizing the parameters of a model. The concept is then expanded both vertically and horizontally. The vertical expansion includes the introduction of levels and categories. The horizontal expansion includes the incorporation of several architectures of a single model as well as separate models.

Chapter 2

Optical Buses

2.1 Introduction

The computer bus is the communications path between internal components of the computer. It is usually a shared, physical medium. The most common bus architecture used today is the electrical bus. Electrical buses have several distinct characteristics including the fact that signal propagation is generally bi-directional and that a processor must be able to obtain exclusive write access to the bus for communication [4]. Due to the constrained bandwidth and limited transmission rate of electronic signals, the bus becomes a bottleneck that constrains the processing potential of a multi-processor machine.

The bus needs to be upgraded to support the future speed and bandwidth requirements of a bus-based multi-processor system. Using optical bus interconnections is a proposal that builds upon known aspects of existing optical technology. It is known that optical interconnects provide a much larger bandwidth than electronic interconnects, are faster and more processors may be connected via optics [5]. Optical networks are also less prone to clock skew when connecting a large number of proces-