# EFFECTS OF OFFSETS ON STRESSES OF A SILICON CHIP MOUNTED ON A COPPER LEAD FRAME

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PREVIEW

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by

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PREVIEW

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TO MY PARENTS

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# CHAPTER 1

# INTRODUCTION

This thesis studies the thermomechanical-induced stresses of silicon chips during their mounting process. This thesis consisted of finite element analyses performed to simulate the stresses developed in silicon chips when they are mounted on copper lead frames at various transverse offsets from the center of copper lead frames.

## 1.1 Background

A rapid technical development in the field of semiconductor products has taken place with advent of very-large-scale integration (VLSI) devices. The VLSI design and processing evolution of the 80's has been accompanied by a corresponding fast change of semiconductor packaging technology. The following section gives a brief background information about Integrated Circuit (IC) Packaging.

### 1.1.1 Packaging of Integrated Circuits

Moisture, contamination, heat, vibration, high magnetic forces, and radiation are daily threats to the continuing operation of an integrated circuit (IC) chip. The encapsulation of the IC in a microelectronic package provides the necessary mechanical and environmental protection, as well as an effective means of heat dissipation [1]. Plastic packaging, glass-sealed ceramic (Cerdip) packaging, and metal-sealed multilayered ceramic (MLC) packaging are the three major packaging technologies in use in today's IC industry [1].



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Encapsulation of IC devices in plastics dates back to 1950 with the advent of the first germanium transistors. Plastics provided a low cost alternative in 1962 with the introduction of plastic encapsulated transistors for the consumer market. A plastic encapsulated IC package is basically a composite structure consisting of relatively brittle materials. The discrepancy between the thermal expansion coefficients of the silicon chip, the metallic lead frame, and the epoxy thermosetting molding compound becomes crucial in a temperature fluctuating environment. Large normal and shear stresses can develop in the molding compound and the silicon chip. Such thermal stresses may tend to be severe enough to cause fracturing in either material during the thermal cycling [2] in the manufacturing process.

Early encapsulants based on silicon, epoxy anhydride and phenolic resins lacked desirable moisture and thermal cycling performance [3]. By 1972, the epoxy/novalac system became the encapsulant of choice. In 1982, the silicon-modified epoxy/novalac system was introduced. The new system resulted in low stresses transmitted to the die surface and in an improvement of the mechanical characteristics of the package by limiting crack propagation propensity [3]. To reduce the stresses in the molded plastic package, the mechanical mismatch at interfaces has to be reduced through lowering the coefficient of thermal expansion and by making the encapsulant more compliant by reducing the elastic modulus. As the values of these two quantities of the molding compound approaches that of the other materials of construction in the package (silicon chip, metal lead frame, etc.), the mechanical stresses due to the material differences

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decrease [3]. Improvements in the interest of providing a lowered stress environment in the molded plastic package now are pursued principally through modifications in the resin chemistry. The effect of shear stress on the die surface can be minimized by decoupling the surface from the molding compound by using a thin compliant coating [3].

## 1.2 Nature of the Problem

The silicon chip is normally bonded to a metallic lead frame using an epoxy at the temperature that optimizes the curing of the epoxy.The entire unit is cooled to room temperature for test and use. This cooling causes stresses to build up between the silicon chip and the lead frame because of the difference in the thermal expansion coefficients. The silicon chip and metallic lead frame form a bimetallic plate in the region where they are bonded together. This bimetallic plate will try to bow in a concave downward sense when the package is cooled. A typical silicon chip contains P-Silicon layer, N- Silicon layer and a protective coating layer. A material is said to be N-type because the current carriers are negative charges. In N-type material electrons are referred to as majority carriers and the holes as minority carriers. In P-type material the positive holes are responsible for most of the current. The IC circuit is usually located in the N-type layer.

This is a steady state problem where stresses are introduced by thermal loads. This problem can be solved as a bimetallic plate problem with the epoxy as a glue layer. In this approach, the silicon chip, epoxy, and metallic lead frame would be bonded together at epoxy curing temperature in a stress free condition and then cooled to room temperature to evaluate the stresses in the chip. The only stresses that are of particular

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interest are those in the N-type layer. Determination of the effect on the stresses to the kind of dimensional tolerances that are likely to be encountered in the assembly of the first level IC packaging are of particular importance. If the chip is at the center of the lead frame, the pattern and magnitude of the stresses will be symmetric about the center of the chip. If the silicon chip is at an offset with respect to the center of the lead frame, the pattern and magnitude of the stresses will be non-symmetric about the center of the chip.

### 1.3 Objectives of Analyses

The aim of this study is to quantitatively determine the distribution and magnitude of stresses introduced into a silicon chip when the chip is mounted on the lead frame with offsets from the center. The objectives of this study can be summarized with the following two facts:

1). Determine the magnitude and distribution of stresses in the N-type layer when the silicon chip is at an offset with respect to the center of the lead frame.

2). Develop equations that predict the magnitude of the stresses within the center region of the chip for any offset of the chip from the center of the lead frame.

### 1.4 Scope of Study

The purpose of this study is to evaluate the stress introduced into the silicon chip when it is bonded to a nonmagnetic (copper) lead frame with a conductive epoxy. It is assumed that the proper application of plastic overcoat will isolate the die

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from stresses introduced by the injection-molded epoxy used in the body of the package. The overcoat issue is not addressed in this study. However, the results of this study are not expected to be significantly impacted by the subsequent molding of the plastic package around the lead frame and the die when the die and part of the top surface of the lead frame are properly coated. The stress effect of unsymmetrical leads extending from the copper flag are also not addressed in this study.

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# CHAPTER 2

# TYPICAL MANUFACTURING PROCESS OF SILICON CHIPS

## 2.1 Wafer Preparation

Typical chips are manufactured from 3-inch or 4-inch diameter silicon wafers of a typical thickness of 15 mils (0.381 mm). The completed wafers have various epitaxial layers and impurity diffusions on the front and back surfaces to form the resistors, capacitors, and transistors needed to meet functional requirements. The impurity elements are usually present in parts per million or less and do not significantly change the Young's modulus or the temperature coefficient of the materials. However, the impurity elements do introduce stresses into the single crystal silicon lattice which causes the wafers to bow in a concave downward manner to give a rise of a few mils at the center of the wafers.

The top surface of the wafers are then coated with protective coating layers which are deposited at the curing temperature of that particular coating material. These layers are key to the protection and passivation of the clean oxides and metal layers on the surface of the wafers. The coefficient of thermal expansion of that protective layers will be different than that of the wafers. As a result, when the wafers cool down to room temperature, the protective layers are put into tension causing the wafers to bow in a concave downward manner and the center of the wafers rises an additional amount.

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