A GRAPHICS SYSTEM DESIGN BASED ON THE INTEL

82720 GRAPHICS DISPLAY CONTROLLER

APPROVED:

Yu-cheng Liu
Chairman

Raymond Bell

David N Walker

Dean of the Graduate School

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by

CHANGON TSAY, B.E.

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ABSTRACT

This thesis describes the design and implementation of a simple graphics system based on the Intel 82720 graphics display conntroller. The graphics software includes the driver for a iSBX 275 Video Graphics Controller Multimodule board, and a selected set of GKS functions. The design goal was to provide the Intel 310/86 microcomputer with a raster-scan computer graphics system. The GKS standard was chosen to provide the interface between the user's application program and the graphics system.

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Chapter 1

INTRODUCTION

The iSBX 275 Video Graphics Controller (VGC) board [1] is designed to work with a general purpose microprocessor in order to implement a computer graphics system. For this particular implementation, the iSBX 275 VGC board is connected to the Intel 310/86 microcomputer through the standard eight-bit iSBX bus connector [5] and is used to generate the basic video signals to the video display monitor. The host processor passes commands and data to the iSBX 275 VGC board through the iSBX bus. Upon receipt of the commands, the iSBX 275 VGC board performs all the tasks needed to manage the display memory.

Commands sent to the iSBX 275 VGC board consist of a series of instructions and their associated parameters. The commands and their associated parameters are used to draw a geometric figure or a graphics character into the display memory. The geometric figure or graphics character drawn in the display memory can then be displayed on the monitor. The drawing commands for the iSBX 275 VGC board include the commands for drawing lines, arcs, circles, rectangles, and rectangular area filling. Commands are also available to allow the user to select line styles and patterns for the

figures that are to be drawn into the display memory.

The host processor, under control of the graphics software program, performs the preliminary calculations to prepare the drawing parameters, and provides the starting point into the display memory and other associated parameters of the figure to be drawn. The iSBX 275 VGC calculates the display memory addresses bit-by-bit for the graphics figure to be drawn and completes the drawing without further intervention from the host processor.

1.2 Functional Description of The iSBX 275 VGC Board

The iSBX 275 VGC board is composed of five logical blocks as shown in Figure 1-1. These five logical blocks of the iSBX 275 VGC board are:

(1) Graphic Display Controller.
(2) Control Logic.
(3) Clock Generator.
(4) Display Memory.
(5) Shift Register and Output Buffer.

The heart of the iSBX 275 VGC board is the Intel 82720 Graphic Display Controller (GDC) chip [2,3]. The GDC is an intelligent microprocessor peripheral chip designed as a raster-scan computer graphics controller. The control of the GDC by the host processor is achieved through the stan-

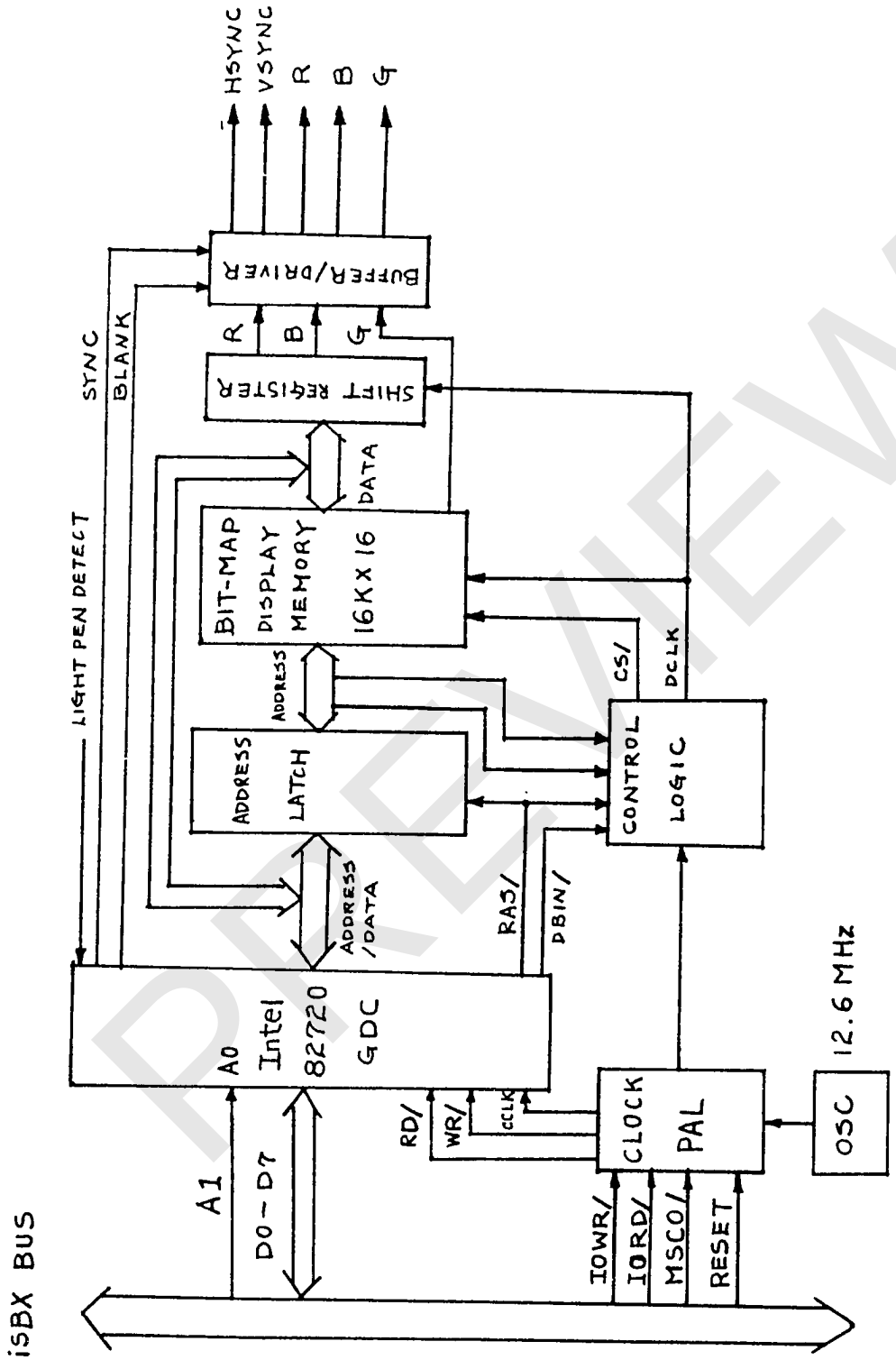

Figure 1-1 The block diagram of the iSBX 275 VGC board.

dard eight-bit bi-directional iSBX bus interface. The access to the GDC is coordinated through the flags in the status register which resides in the GDC. The bi-directional iSBX bus interface allows the host processor to send command and parameters to the GDC. The flags in the status register concerning the drawing process of the iSBX 275 VGC board is read by the host processor before each read or write operation to the GDC.

The First In First Out (FIFO) buffer in the GDC serves as an interface to the iSBX bus. Through this FIFO, commands and data sent by the host processor can be accessed by the GDC and data requested by the host processor can be read. Access to the 16-byte FIFO is controlled by the host processor through the GDC's command set. The host processor coordinates the transfers by checking the appropriate status register bits. Commands and parameter bytes are sent to the GDC's FIFO and are differentiated based on the state of the system address bit A1. When the write control line is activated, the GDC configures the FIFO as an input buffer to receive the command and the parameter bytes from the host processor. If a read command is issued to the GDC, the GDC interprets the command, configures the FIFO as an output buffer and places the requested data into the FIFO. A flag in the status register indicates that the data are ready to be retrieved. The host processor can then retrieve the re-

quested information by activating the read control line.

When the host processor sends a command byte and activates the write control line (IOWR/) to the GDC, the GDC treats the data written into the FIFO as a command. The GDC decodes the command, distributes the succeeding parameter bytes to the proper registers within the GDC, and then initiates the required operation.

The host processor, under the software control, programs the GDC sync logic during initialization with either a RESET or a SYNC command and the associated parameters. The GDC generates the sync signals (horizontal and vertical) as well as the blanking signals to the attached monitor for any interlaced or non-interlaced video format.

The clock generator consists of a crystal oscillator and a clock programmable array logic (PAL) chip. Together, they provide the timing signals for GDC. The dot frequency which determines the speed of the bit-map display, may be the oscillator frequency or the oscillator frequency divided by two (jumper selectable). The frequency selected must provide a dot frequency of at least 4 MHZ and less than 13 MHZ for a monochrome monitor and less than 10 MHZ for a color monitor.

The clock PAL decodes the control lines IORD/, IOWR/, and MCS0/ sent by the host processor, and generates an RD/

or WR/ signal to the GDC. The iSBX 275 VGC board does not support DMA transfers.

The control logic consists of a control PAL which aids the GDC in controlling access to the display memory. There are two types of accesses to the display memory: the display cycle, and the read-modify-write (RMW) cycle. During a display cycle, the data at the addressed location are read and sent to the shift register for subsequent display on the monitor. During an RMW cycle, data are accessed from the display memory, modified, and written back into the display memory. The modifications that can be performed to the data at the addressed location are complement, set, clear, and replace.

The display memory consists of sixteen 16K x 1 static RAMs which provide 16K words with each having 16 bits. The address of the display memory is calculated by the GDC and latched in the address latch. The data stored at the addressed location may be modified by the GDC, passed back to the host processor, or displayed on the monitor. When using a black-and-white monitor, all of the display memory is accessible. On the other hand, if a color monitor is used, one block (1/4) of the display memory is available for each of the colors: red, blue and green. When the data stored at the addressed RAM location are to be displayed, they are loaded in parallel into the shift register and then output

in serial to the monitor at the rate of the dot frequency.

The shift register logic consists of three 16-bit registers (one for each color) and a series of D flip-flops. Each shift register performs the parallel-to -serial conversion that produces the video bit-stream sent to the attached monitor. The additional D-type flip-flops are used to resynchronize the video data with the synchronizing signals and blanking signals output to the connector. If the GDC is programmed in black-and-white mode, only one shift register is used.

1.3 Hardware Interface for The TV Monitor

Since the video outputs of the iSBX 275 VGC board are TTL signals [1], a special interface circuit is designed so that a standard TV set can be used as a monitor. In Figure 1-2, the MC1377 chip [7] serves as an encoder and is used to combine the RGB video signals and the sync signal of the iSBX 275 VGC board and to convert them to the analog TV signal. The converted video signal is then fed into the RF modulator. The output of the modulator is connected to the antenna input of a TV set. Because two special components (TOK0166NNF/10264AG and 400 ns Y Delay line) are required and we were unable to obtain these devices, only the monochrome picture can be produced by using this circuit.

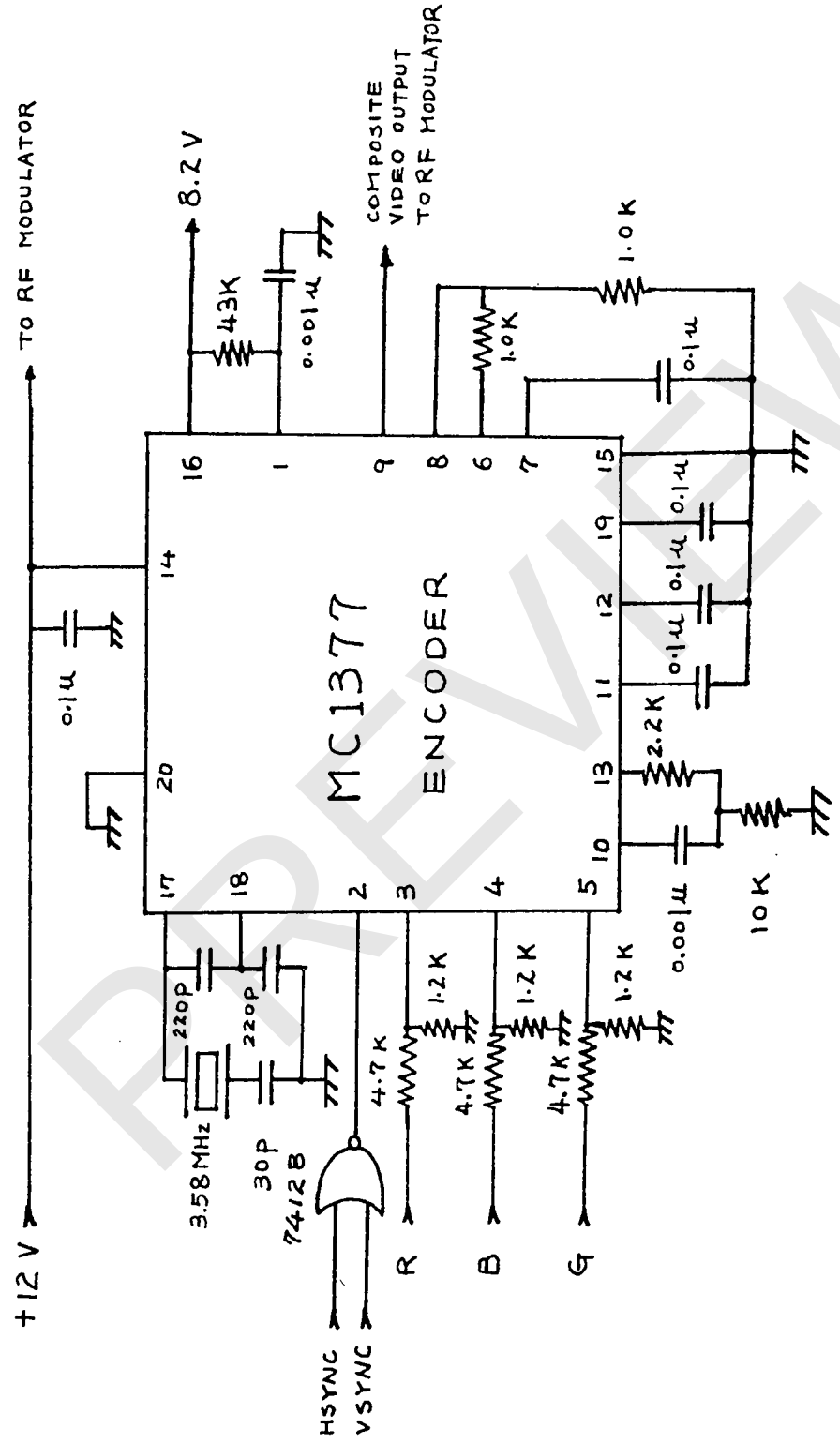

Figure 1-2 The TV interface circuit.

Chapter 2

PROGRAMMING INFORMATION

2.1 General Description

This chapter discusses the access of the iSBX 275 VGC board, the on-board display memory, and the commands that are available to the programmer. The different modifications to the display memory that can be performed in an RMW cycle by the GDC are also discussed.

2.2 Addressing

The iSBX 275 VGC board is accessed in the I/O space of the host processor by using input and output instructions. For the Intel system 310/86, the addresses associated with the iSBX bus connector J4 and J3 are 80H through 9EH, and A0H through BEH, respectively [5]. The iSBX 275 VGC board is connected to J4, and Figure 2-1 shows the register address of the iSBX 275 VGC board.

A1	A0	Address	GDC Register
0	0	80H	command/status
1	0	82H	data

Figure 2-1 The register address of the iSBX 275 VGC board.

The GDC uses system address pin A1 to distinguish commands from parameters that are received from the host. Before data or commands are written from the host processor to the iSBX 275 VGC board, the host processor should check the status register to ensure that the FIFO is not full. The format of the status register is shown in Figure 2-2 and the definition of each bit is given below.

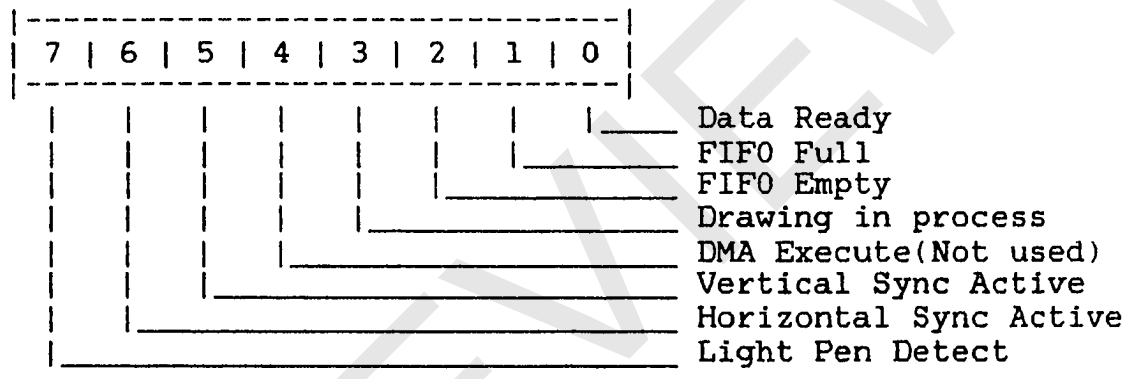

Figure 2-2 The format of the status register.

Data Ready - When this flag is set to 1, it indicates that a byte is available to be read by the microprocessor. The data ready bit must be tested before each read operation by the system microprocessor. The flag is reset after the data is transferred from the FIFO into the microprocessor.

FIFO Full - When this flag is set to 1, it indicates that the FIFO is full. A value of 0 ensures that there is room for at least one more byte. This flag must be checked before each write into the GDC.

FIFO Empty - This flag and the FIFO full flag coordinate the system microprocessor's accesses of the GDC's FIFO. When it contains a 1, the empty flag ensures that all the commands and parameters previously sent to the GDC have been processed.

Drawing in Progress - This status flag is set to 1 while the GDC is drawing a graphics figure.

DMA Execute - This bit is a 0 since DMA is not supported.

Vertical Sync Active - This flag is a 1 during vertical retrace. The vertical flag coordinates display-format-modifying commands to the blanked interval surrounding the vertical sync. This eliminates display disturbances.

Horizontal Sync Active - A value of 1 for this flag signifies that horizontal retrace blanking is currently underway.

Light Pen Detect - When this bit is set to 1, the light pen address (LAD) register contains a value (word address) that the system microprocessor can read. This flag is reset after the three bytes of the LAD are moved into the FIFO in response to the light pen read command.

2.3 Display Memory Organization

The on-board bit-map display memory consists of 16K words of 16 bits each beginning at address 0 to the GDC.

For a display operation, the GDC reads a word from the memory during each cycle, and displays it on the screen starting at the top left corner, and sequenceing down toward the bottom right corner. Because the display memory is read a word at a time, the display resolution in the horizontal direction must be a multiple of 16. The least significant bit of a word is displayed first. The GDC chip has a total of 18 address bits, but the iSBX 275 VGC board only uses the least 14 significant bits. The upper address bits from the GDC are ignored.

When in black-and-white mode, all 16K words of the display memory are in a contiguous block which may be written to and displayed. A 1 written into the bit-map is displayed as an illuminated dot.

When the iSBX 275 VGC board is programmed in color mode, three color planes exist sequentially in memory, but are displayed simultaneously. The planes are each 4K words long and are in the order of red, blue, and green. The red plane starts at the memory address 0, the blue plane at the memory address 1000H, and the green plane at the memory address 2000H. A 1 written into a given plane illuminates the corresponding color dot. Table 2-1 lists the color plane combinations for the various colors. If a figure is to be drawn in a color that is composed of two or more primary colors, the GDC must be programmed to draw the figure

separately for each color plane. This is done by changing the cursor base address and repeating the drawing command and parameters.

Color plane			Displayed Color
Green	Blue	Red	
0	0	0	Black
0	0	1	Red
0	1	0	Blue
0	1	1	Magenta
1	0	0	Green
1	0	1	Yellow
1	1	0	Cyan
1	1	1	White

Table 2-1 The color plane combinations.

2.4 Command Summary

The GDC commands [1,3] are organized into four categories: video control commands, display control commands, drawing control commands, and data read commands. They are summarized below.

Video Control Commands

RESET	00H
VSYNC	6FH
SYNC	0FH (0EH)

Display Control Commands

PITCH	47H
ZOOM	46H
CURS	49H
PRAM	7XH
START	6BH
BCTRL	0CH (0DH)

Drawing Control Commands

FIGS	4CH
MASK	4AH
FIGD	6CH
GCHRD	68H

Memory Data Read Commands

WDAT	20H (21H, 22H, 23H)
RDAT	A0H (A1H, A2H, A3H) (Not used)
CURD	E0H (Not used)
LPRD	C0H (Not used)

2.5 Video Control Commands

The video control commands are used to initialize the iSBX 275 VGC board after a power-up sequence. Normally, these commands need not be repeated after being executed once.

RESET command (00H) - This command is used to initialize the operation and display modes of the GDC. It resets