

INFORMATION TO USERS

This dissertation copy was prepared from a negative microfilm created and inspected by the school granting the degree. We are using this film without further inspection or change. If there are any questions about the content, please write directly to the school. The quality of this reproduction is heavily dependent upon the quality of the original material.

The following explanation of techniques is provided to help clarify notations which may appear on this reproduction.

1. Manuscripts may not always be complete. When it is not possible to obtain missing pages, a note appears to indicate this.
2. When copyrighted materials are removed from the manuscript, a note appears to indicate this.
3. Oversize materials (maps, drawings and charts are photographed by sectioning the original, beginning at the upper left hand corner and continuing from left to right in equal sections with small overlaps.

UMI[®]

ProQuest Information and Learning
300 North Zeeb Road, Ann Arbor, MI 48106-1346 USA
800-521-0600

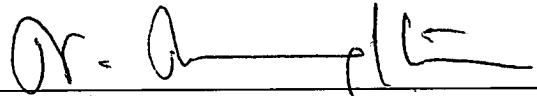
PREVIEW

AN ALGORITHM TO PARTITION DESIGNS FOR DELAY-DRIVEN
SCHEDULING ON A TIME-MULTIPLEXED FIELD PROGRAMMABLE GATE
ARRAY

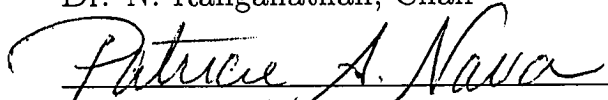
ADARSH PANIKKAR

Electrical and Computer Engineering Department

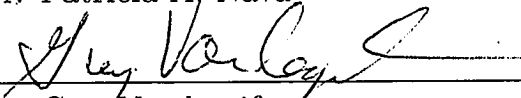
APPROVED:



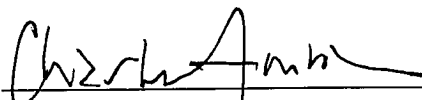
Dr. N. Ranganathan, Chair



Dr. Patricia A. Nava



Dr. Guy Vandegrift



Associate Vice President
for Graduate Studies

AN ALGORITHM TO PARTITION DESIGNS FOR DELAY-DRIVEN
SCHEDULING ON A TIME-MULTIPLEXED FIELD PROGRAMMABLE GATE
ARRAY

by

ADARSH PANIKKAR, B. E.

THESIS

Presented to the Faculty of the Graduate School of

The University of Texas at El Paso

in Partial Fullfillment

of the Requirements

for the Degree of

MASTER OF SCIENCE

Electrical and Computer Engineering Department

THE UNIVERSITY OF TEXAS AT EL PASO

July, 1999

This work is dedicated to metal god Judas Priest, the power and majesty of whose music has "guided me so bright".

PREVIEW

Acknowledgements

I wish to express my gratitude to Dr. N Ranganathan, the committee chair, for being my guide in all respects of education and research. He has been a constant source of motivation at all times during this research. I would like to thank Dr. Abdel Ejnoui for his valuable guidance and encouragement. But for his keen interest and support, this thesis would not have taken the present form.

I would like to thank my committee members for their suggestions and comments.

I am immensely indebted to Ashok Murugavel, my research teammate for all his valuable suggestions, and help extended during the drafting of this work. I also wish to express my gratitude to my friends Pritam and Ganesh for helping me and being with me under all circumstances, to Ricardo Mesta and Hugo Garcia for help extended during the coding of the algorithm, to Leopoldo, my colleague at the computer lab for his support during the course of this research, to Bharath and Pramod for their support and cooperation.

Abstract

Field Programmable Gate Arrays (FPGAs) provide logic, storage and interconnect elements in a standard component that can be configured at run time to function as an application specific part. Recently, the time-multiplexed FPGA architecture is being investigated as a solution to handle large circuits that cannot be mapped onto a single FPGA chip. The large circuit is partitioned and executed on the single FPGA architecture in a sequential manner. This thesis addresses the problem of delay-driven scheduling of a large design onto a time-multiplexed FPGA. An acyclic graph corresponding to the circuit to be scheduled is generated, and the algorithm schedules nodes satisfying the precedence and assignment constraints and prioritizes by scheduling the larger paths first. The results obtained for scheduling MCNC' 93 circuits show that the proposed algorithm yields optimal number of partitions with the minimal total delay.

Contents

| | |
|---|-------------|
| Acknowledgements | iv |
| Abstract | v |
| List of Figures | viii |
| List of Tables | ix |
| 1 Introduction | 1 |
| 1.1 Need for FPGAs | 2 |
| 1.2 FPGA Architecture | 3 |
| 1.3 Time-Multiplexed FPGA | 5 |
| 1.3.1 Trimberger Architecture | 5 |
| 1.3.2 Modes of Operation | 7 |
| 1.4 Design scheduling in a Time-Multiplexed FPGA | 8 |
| 1.5 Thesis Contribution | 10 |
| 1.6 Thesis Overview | 11 |
| 2 Related Work | 12 |
| 2.1 The Optimizing Scheduler by Trimberger | 13 |
| 2.1.1 Levelized Scheduling | 14 |

2.1.2 The Optimizing Scheduler 15

2.2 Circuit Scheduler by Ejnoui and Ranganathan 18

3 Proposed Solution 22

3.1 Problem Statement 23

3.2 Preliminaries 27

3.3 Problem formulation 28

3.4 Proposed Solution 29

4 Experimental Results 36

5 Conclusions 40

References 42

Curriculum Vitae 45

PREVIEW

List of Figures

| | | |
|-----|--|----|
| 1.1 | Architecture of FPGAs [2] | 3 |
| 1.2 | Configuration of FPGA blocks and interconnections by configuration memory [2] | 4 |
| 1.3 | Configuration model of a time-multiplexed FPGA [6] | 6 |
| 1.4 | Logic Engine Model [6] | 8 |
| 1.5 | Architecture of the time-multiplexed FPGA [6] | 9 |
| 2.1 | Scheduling Leeway for a Representative Design [9] | 15 |
| 2.2 | Schedule of flow graph of a virtual design for a resource constraint of 3 | 21 |
| 3.1 | A technology mapped virtual design | 24 |
| 3.2 | A technology mapped virtual design | 24 |
| 3.3 | Possibility 1 of scheduling virtual design with a resource constraint of 4 (Schedule 1) | 25 |
| 3.4 | Possibility 2 of scheduling virtual design with a resource constraint of 4 (Schedule 2) | 25 |
| 3.5 | Acyclic flow graph of virtual design shown in fig 3.1 | 28 |
| 3.6 | Example of a situation where total delay is more than optimal | 33 |
| 3.7 | Schedule of flow graph of a virtual design for a resource constraint of 3 | 35 |

List of Tables

| | | |
|-----|--|----|
| 4.1 | MCNC'93 circuits | 36 |
| 4.2 | Results of the Scheduling Algorithm | 37 |
| 4.3 | Path Compression Results of the Scheduling Algorithm | 38 |

PREVIEW

Chapter 1

Introduction

Ever since the invention of the Programmable Array Logic (PAL) device at Monolithic Memories in 1978, Programmable Logic Devices (PLDs) have been popular, and have evolved considerably. Programmable logic devices provide a solution to the shortcomings of discrete TTL logic. The use of programmable logic has become much easier with the availability of design software. The fact that designers do not have to be worried about low-level implementation issues with these devices has made it possible to design complex circuits with reduced design cycle times.

A programmable logic device can be defined as one with configurable logic and storage elements, linked together by a programmable interconnect. The configuration of the logic devices, and interconnection between the various functions are decided by memory cells present in the device. Most of the devices, though may employ different architectures, are based upon this idea.

Some of the major programmable architectures available today are

- Simple Programmable Logic Devices-**SPLDs** also known as PAL (Programmable Array Logic), GAL (Generic Array Logic), PLA (Programmable Logic Array) or PLD (Programmable Logic Device)

Can typically replace a few 7400-series TTL devices. Each macrocell within