AN ALGORITHM TO PARTITION DESIGNS FOR DELAY-DRIVEN SCHEDULING ON A TIME-MULTIPLEXED FIELD PROGRAMMABLE GATE ARRAY

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This work is dedicated to metal god Judas Priest, the power and majesty of whose music has "guided me so bright".

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Abstract

Field Programmable Gate Arrays (FPGAs) provide logic, storage and interconnect elements in a standard component that can be configured at run time to function as an application specific part. Recently, the time-multiplexed FPGA architecture is being investigated as a solution to handle large circuits that cannot be mapped onto a single FPGA chip. The large circuit is partitioned and executed on the single FPGA architecture in a sequential manner. This thesis addresses the problem of delay-driven scheduling of a large design onto a time-multiplexed FPGA. An acyclic graph corresponding to the circuit to be scheduled is generated, and the algorithm schedules nodes satisfying the precedence and assignment constraints and prioritizes by scheduling the larger paths first. The results obtained for scheduling MCNC' 93 circuits show that the proposed algorithm yields optimal number of partitions with the minimal total delay.

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Chapter 1

Introduction

Ever since the invention of the Programmable Array Logic (PAL) device at Monolithic Memories in 1978, Programmable Logic Devices (PLDs) have been popular, and have evolved considerably. Programmable logic devices provide a solution to the short comings of discrete TTL logic. The use of programmable logic has become much easier with the availability of design software. The fact that designers do not have to be worried about low-level implementation issues with these devices has made it possible to design complex circuits with reduced design cycle times.

A programmable logic device can be defined as one with configurable logic and storage elements, linked together by a programmable interconnect. The configuration of the logic devices, and interconnection between the various functions are decided by memory cells present in the device. Most of the devices, though may employ different architectures, are based upon this idea.

Some of the major programmable architectures available today are

- Simple Programmable Logic Devices-**SPLDs** also known as PAL (Programmable Array Logic), GAL (Generic Array Logic), PLA (Programmable Logic Array) or PLD (Programmable Logic Device)

  Can typically replace a few 7400-series TTL devices. Each macrocell within